Data Sheet May 2, 2007 FN7046.4

Ultra-Low Noise, Low Power, Wideband Amplifier

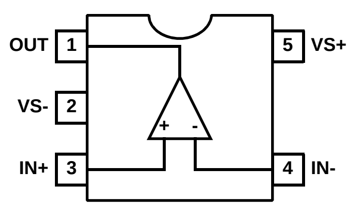
The EL2126 is an ultra-low noise, wideband amplifier that runs on half the supply current of competitive parts. It is intended for use in systems such as ultrasound imaging where a very small signal needs to be amplified by a large amount without adding significant noise. Its low power dissipation enables it to be packaged in the tiny SOT-23 package, which further helps systems where many input channels create both space and power dissipation problems.

The EL2126 is stable for gains of 10 and greater and uses traditional voltage feedback. This allows the use of reactive elements in the feedback loop, a common requirement for many filter topologies. It operates from ±2.5V to ±15V supplies and is available in the 5 Ld SOT-23 and 8 Ld SO packages.

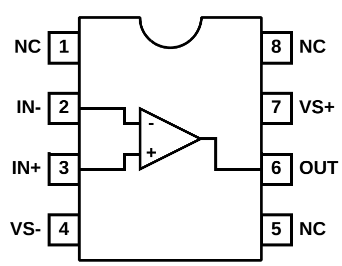
The EL2126 is fabricated in Elantec's proprietary complementary bipolar process, and is specified for operation over the full -40°C to +85°C temperature range.

Pinouts

EL2126
(5 LD SOT-23)
TOP VIEW



EL2126
(8 LD SOIC)
TOP VIEW



Features

- Voltage noise of only 1.3nV/√Hz
- Current noise of only 1.2pA/√Hz
- 200µV offset voltage
- 100MHz -3dB BW for A_V = 10
- Very low supply current - 4.7mA
- SOT-23 package
- ±2.5V to ±15V operation
- Pb-free plus anneal available (RoHS compliant)

Applications

- Ultrasound input amplifiers
- Wideband instrumentation
- Communication equipment
- AGC and PLL active filters
- Wideband sensors

Ordering Information

PART NUMBER	PART MARKING	TEMP RANGE (°C)	TAPE AND REEL	PACKAGE	PKG. DWG. #
EL2126CW-T7	G	-40 to +85	7” (3k pcs)	5 Ld SOT-23	MDP0038
EL2126CW-T7A	G	-40 to +85	7” (250 pcs)	5 Ld SOT-23	MDP0038
EL2126CS	2126CS	-40 to +85	-	8 Ld SOIC (150 mil)	MDP0027
EL2126CS-T7	2126CS	-40 to +85	7”	8 Ld SOIC (150 mil)	MDP0027
EL2126CS-T13	2126CS	-40 to +85	13”	8 Ld SOIC (150 mil)	MDP0027
EL2126CSZ (Note)	2126CSZ	-40 to +85	-	8 Ld SOIC (150 mil) (Pb-free)	MDP0027
EL2126CSZ-T7 (Note)	2126CSZ	-40 to +85	7”	8 Ld SOIC (150 mil) (Pb-free)	MDP0027
EL2126CSZ-T13 (Note)	2126CSZ	-40 to +85	13”	8 Ld SOIC (150 mil) (Pb-free)	MDP0027
EL2126CWZ-T7 (Note)	BAAH	-40 to +85	7”	5 Ld SOT-23 (SC74) (1.65mm) (Green)	P5.064
EL2126CWZ-T7A (Note)	BAAH	-40 to +85	7”	5 Ld SOT-23 (SC74) (1.65mm) (Green)	P5.064

NOTE: Intersil Pb-free products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Absolute Maximum Ratings

V_S+ to V_S-) 33V
Continuous Output Current 40mA
Any Input . . . . V_S+ -0.3V to V_S- +0.3V

Thermal Information

Operating Temperature . . . . -40°C to +85°C
Storage Temperature . . . . -60°C to +150°C
Maximum Die Junction Temperature . . . . +150°C
Power Dissipation . . . . See Curves
Pb-free reflow profile . . . . see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

Electrical Specifications

V_S+ = +5V, V_S- = -5V, T_A = +25°C, R_F = 180Ω, R_G = 20Ω, R_L = 500Ω Unless Otherwise Specified.

Parameter	Description	Conditions	Min	Typ	Max	Unit
DC PERFORMANCE						
V_{OS}	Input Offset Voltage (SO8)			0.2	2	mV
	Input Offset Voltage (SOT23-5)				3	mV
T_{CVOS}	Offset Voltage Temperature Coefficient			17		µV/°C
I_B	Input Bias Current		-10	-7		µA
I_{OS}	Input Bias Current Offset			0.06	0.6	µA
T_{CIB}	Input Bias Current Temperature Coefficient			0.013		µA/°C
C_{IN}	Input Capacitance			2.2		pF
A_{VOL}	Open Loop Gain	V_O = -2.5V to +2.5V	80	87		dB
PSRR	Power Supply Rejection Ratio (Note 1)		80	100		dB
CMRR	Common Mode Rejection Ratio	at CMIR	75	106		dB
CMIR	Common Mode Input Range		-4.6		3.8	V
V_{OUTH}	Positive Output Voltage Swing	No load, R_F = 1kΩ	3.8	3.8		V
V_{OUTL}	Negative Output Voltage Swing	No load, R_F = 1kΩ		-4	-3.9	V
V_{OUTH2}	Positive Output Voltage Swing	R_L = 100Ω	3.2	3.45		V
V_{OUTL2}	Negative Output Voltage Swing	R_L = 100Ω		-3.5	-3.2	V
I_{OUT}	Output Short Circuit Current (Note 2)		80	100		mA
I_{SY}	Supply Current			4.7	5.5	mA
AC PERFORMANCE - R_G = 20Ω, C_L = 3pF						
BW	-3dB Bandwidth, R_L = 500Ω			100		MHz
BW ±0.1dB	±0.1dB Bandwidth, R_L = 500Ω			17		MHz
BW ±1dB	±1dB Bandwidth, R_L = 500Ω			80		MHz
Peaking	Peaking, R_L = 500Ω			0.6		dB
SR	Slew Rate	V_{OUT} = 2V_{P-P}, measured at 20% to 80%	80	110		V/µs
OS	Overshoot, 4V_{P-P} Output Square Wave	Positive		2.8		%
		Negative		-7		%
t_S	Settling Time to 0.1% of ±1V Pulse			51		ns

Electrical Specifications
V_S+ = +5V, V_S- = -5V, T_A = +25°C, R_F = 180Ω, R_G = 20Ω, R_L = 500Ω Unless Otherwise Specified.

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_N	Voltage Noise Spectral Density			1.3		nV/√Hz
I_N	Current Noise Spectral Density			1.2		pA/√Hz
HD2	2nd Harmonic Distortion (Note 3)			-70		dBc
HD3	3rd Harmonic Distortion (Note 3)			-70		dBc

NOTES:

1. Measured by moving the supplies from ±4V to ±6V
2. Pulse test only and using a 10Ω load
3. Frequency = 1MHz, V_{OUT} = 2V_{P-P}, into 500Ω and 5pF load

Electrical Specifications
V_S+ = +15V, V_S- = -15V, T_A = 25°C, R_F = 180Ω, R_G = 20Ω, R_L = 500Ω unless otherwise specified.

Parameter	Description	Conditions	Min	Typ	Max	Unit
DC PERFORMANCE						
V_{OS}	Input Offset Voltage (SO8)			0.5	3	mV
	Input Offset Voltage (SOT23-5)				3	mV
T_{CVOS}	Offset Voltage Temperature Coefficient			4.5		µV/°C
I_B	Input Bias Current		-10	-7		µA
I_{OS}	Input Bias Current Offset			0.12	0.7	µA
T_{CIB}	Input Bias Current Temperature Coefficient			0.016		µA/°C
C_{IN}	Input Capacitance			2.2		pF
A_{VOL}	Open Loop Gain		80	90		dB
PSRR	Power Supply Rejection Ratio (Note 4)		65	80		dB
CMRR	Common Mode Rejection Ratio	at CMIR	70	85		dB
CMIR	Common Mode Input Range		-14.6		13.8	V
V_{OUTH}	Positive Output Voltage Swing	No load, R_F = 1kΩ	13.6	13.7		V
V_{OUTL}	Negative Output Voltage Swing	No load, R_F = 1kΩ		-13.8	-13.7	V
V_{OUTH2}	Positive Output Voltage Swing	R_L = 100Ω, R_F = 1kΩ	10.2	11.2		V
V_{OUTL2}	Negative Output Voltage Swing	R_L = 100Ω, R_F = 1kΩ		-10.3	-9.5	V
I_{OUT}	Output Short Circuit Current (Note 5)		140	220		mA
I_{SY}	Supply Current			5	6	mA
AC PERFORMANCE - R_G = 20Ω, C_L = 3pF						
BW	-3dB Bandwidth, R_L = 500Ω			135		MHz
BW ±0.1dB	±0.1dB Bandwidth, R_L = 500Ω			26		MHz
BW ±1dB	±1dB Bandwidth, R_L = 500Ω			60		MHz
Peaking	Peaking, R_L = 500Ω			2.1		dB
SR	Slew Rate (±2.5V Square Wave, Measured 25%-75%)		130	150		V/µS
OS	Overshoot, 4V_{P-P} Output Square Wave	Positive		1.6		%
		Negative		-4.4		%
T_S	Settling Time to 0.1% of ±1V Pulse			48		ns

Electrical Specifications
$V_S+ = +15V$, $V_S- = -15V$, $T_A = 25°C$, $R_F = 180\Omega$, $R_G = 20\Omega$, $R_L = 500\Omega$ unless otherwise specified. **(Continued)**

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_N	Voltage Noise Spectral Density			1.4		nV/√Hz
I_N	Current Noise Spectral Density			1.1		pA/√Hz
HD2	2nd Harmonic Distortion (Note 6)			-72		dBc
HD3	3rd Harmonic Distortion (Note 6)			-73		dBc

NOTES:

4. Measured by moving the supplies from ±13.5V to ±16.5V
5. Pulse test only and using a 10Ω load
6. Frequency = 1MHz, $V_{OUT} = 2V_{P-P}$, into 500Ω and 5pF load

Typical Performance Curves

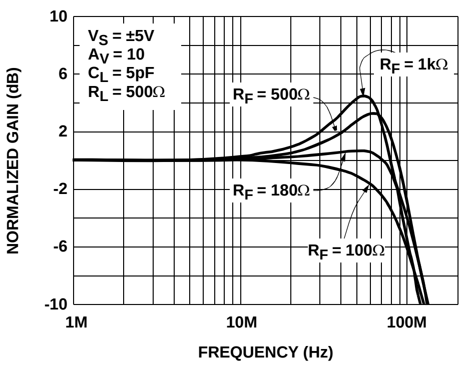


FIGURE 1. NON-INVERTING FREQUENCY RESPONSE FOR VARIOUS RF

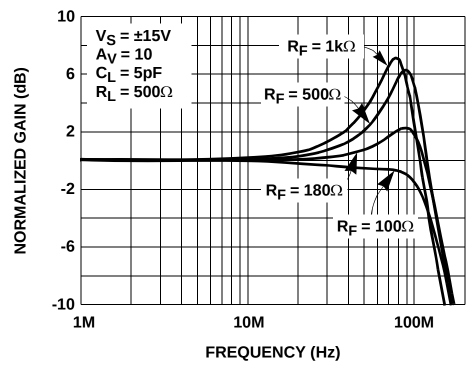


FIGURE 2. NON-INVERTING FREQUENCY RESPONSE FOR VARIOUS RF

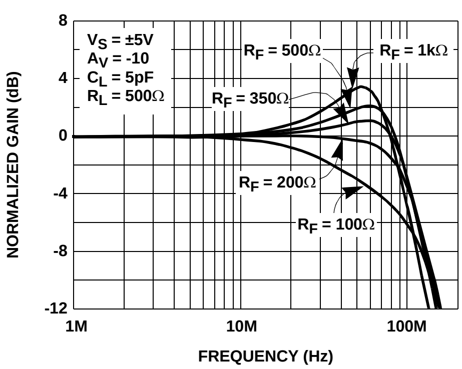


FIGURE 3. INVERTING FREQUENCY RESPONSE FOR VARIOUS RF

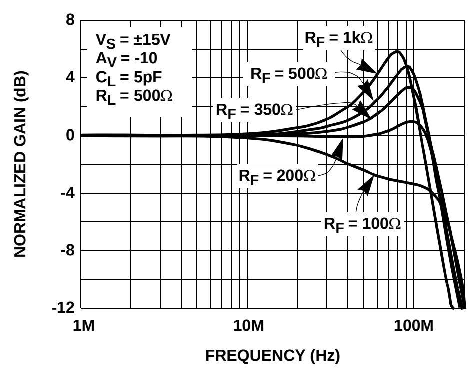


FIGURE 4. INVERTING FREQUENCY RESPONSE FOR VARIOUS RF

Typical Performance Curves (Continued)

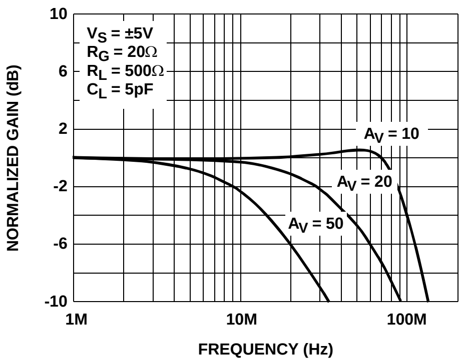


FIGURE 5. NON-INVERTING FREQUENCY RESPONSE FOR VARIOUS GAIN

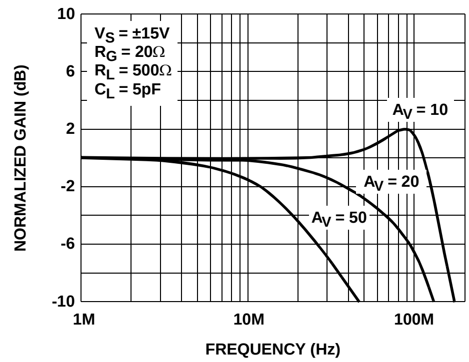


FIGURE 6. NON-INVERTING FREQUENCY RESPONSE FOR VARIOUS GAIN

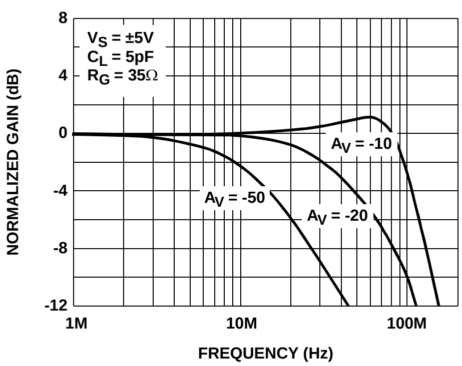


FIGURE 7. INVERTING FREQUENCY RESPONSE FOR VARIOUS GAIN

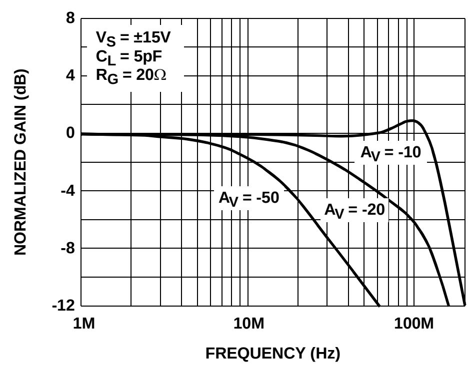


FIGURE 8. INVERTING FREQUENCY RESPONSE FOR VARIOUS RF

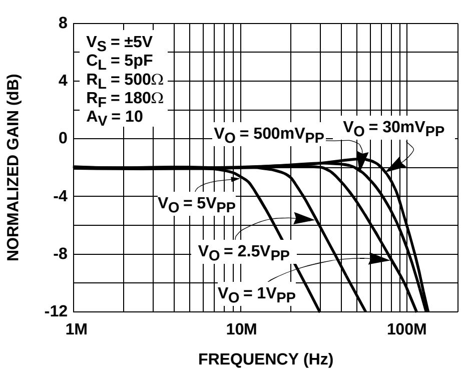


FIGURE 9. NON-INVERTING FREQUENCY RESPONSE FOR VARIOUS OUTPUT SIGNAL LEVELS

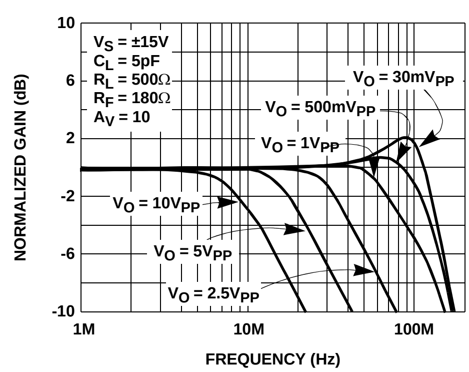


FIGURE 10. NON-INVERTING FREQUENCY RESPONSE FOR VARIOUS OUTPUT SIGNAL LEVELS

Typical Performance Curves (Continued)

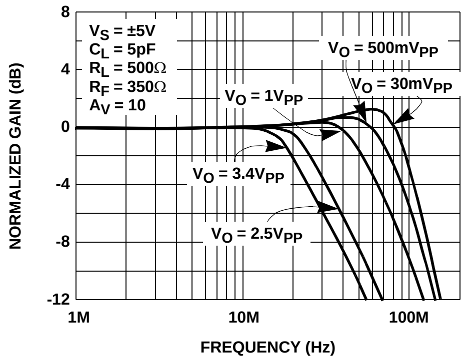


FIGURE 11. INVERTING FREQUENCY RESPONSE FOR VARIOUS OUTPUT SIGNAL LEVELS

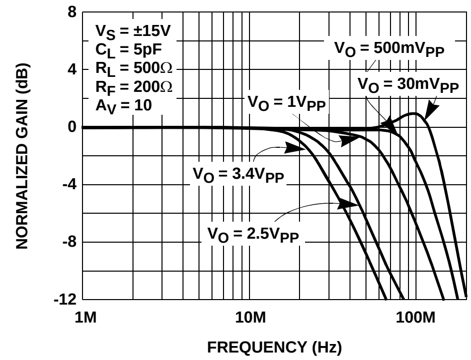


FIGURE 12. INVERTING FREQUENCY RESPONSE FOR VARIOUS OUTPUT SIGNAL LEVELS

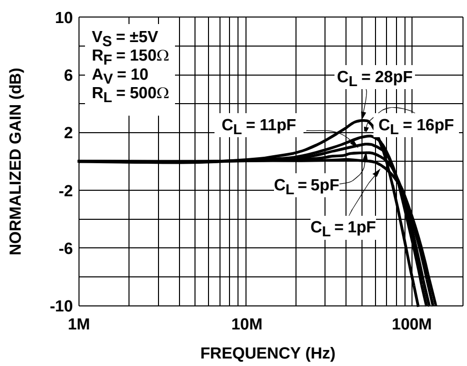


FIGURE 13. NON-INVERTING FREQUENCY RESPONSE FOR VARIOUS CL

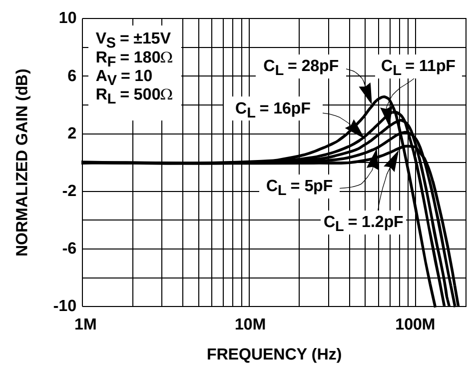


FIGURE 14. NON-INVERTING FREQUENCY RESPONSE FOR VARIOUS CL

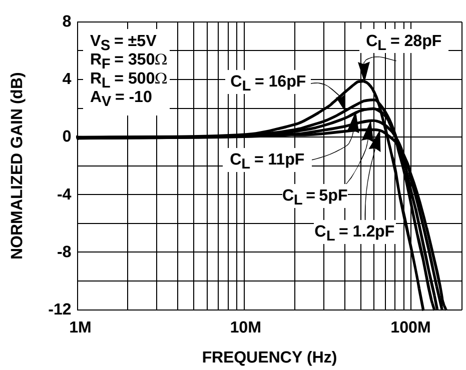


FIGURE 15. INVERTING FREQUENCY RESPONSE FOR VARIOUS CL

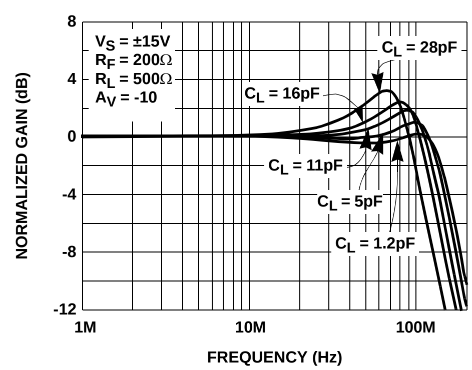


FIGURE 16. INVERTING FREQUENCY RESPONSE FOR VARIOUS CL

Typical Performance Curves (Continued)

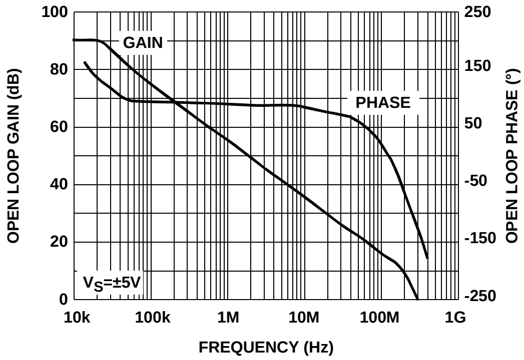


FIGURE 17. OPEN LOOP GAIN AND OPEN LOOP PHASE

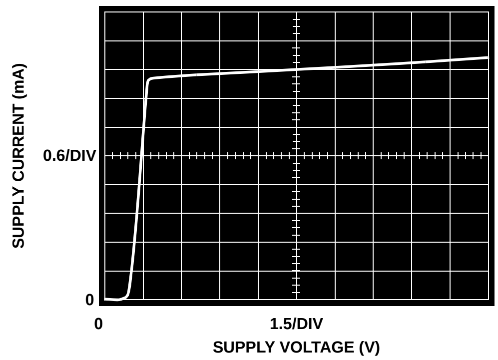


FIGURE 18. SUPPLY CURRENT vs SUPPLY VOLTAGE

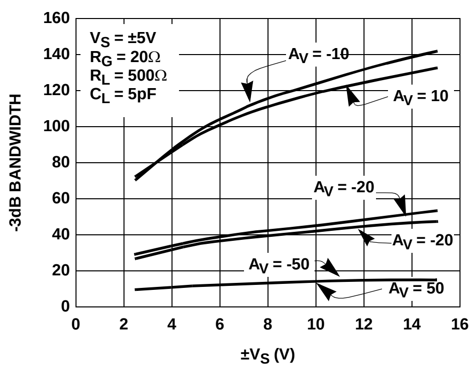


FIGURE 19. BANDWIDTH vs Vs

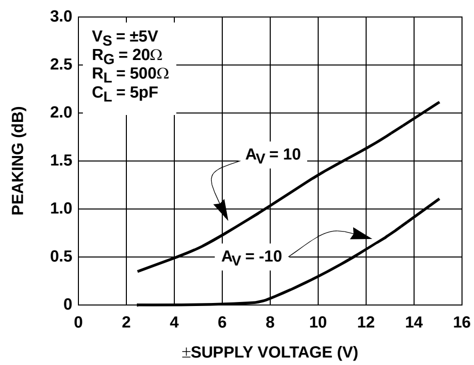


FIGURE 20. PEAKING vs Vs

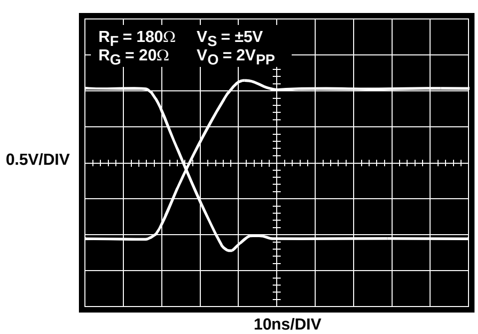


FIGURE 21. LARGE SIGNAL STEP RESPONSE

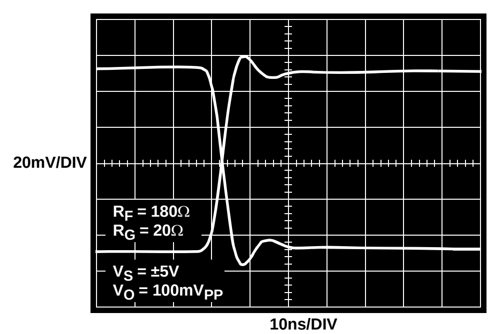


FIGURE 22. SMALL SIGNAL STEP RESPONSE

Typical Performance Curves (Continued)

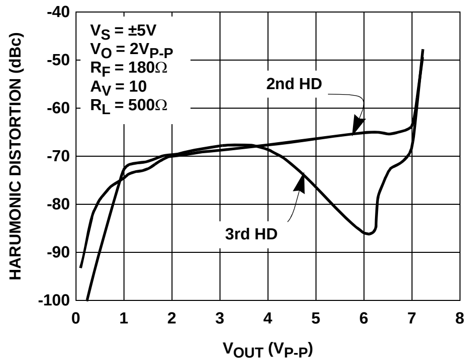


FIGURE 23. 1MHz HARMONIC DISTORTION vs OUTPUT SWING

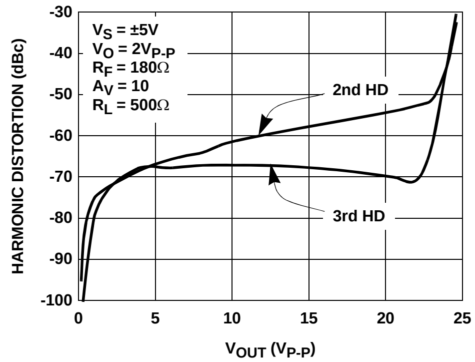


FIGURE 24. 1MHz HARMONIC DISTORTION vs OUTPUT SWING

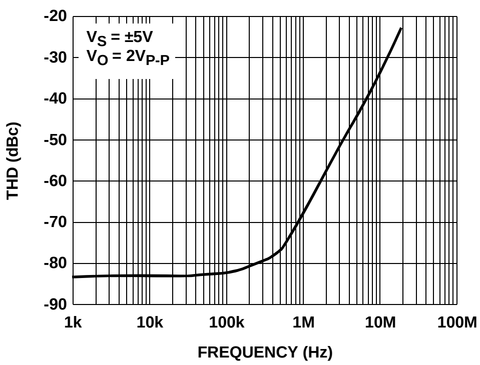


FIGURE 25. TOTAL HARMONIC DISTORTION vs FREQUENCY

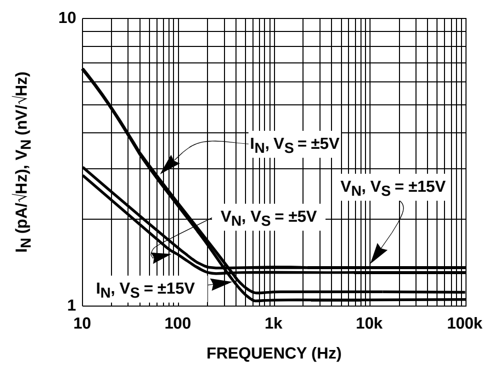


FIGURE 26. NOISE vs FREQUENCY

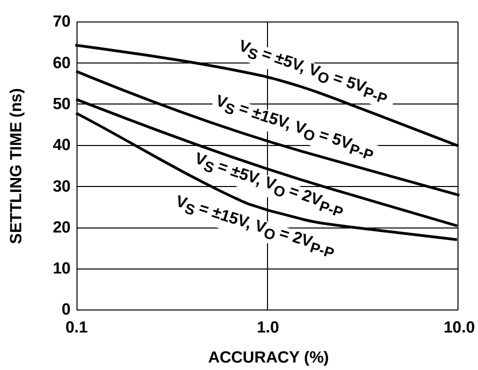


FIGURE 27. SETTLING TIME vs ACCURACY

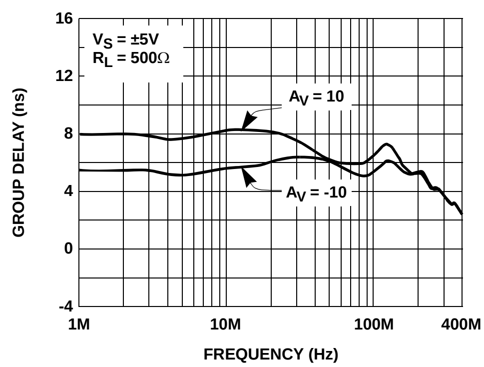


FIGURE 28. GROUP DELAY vs FREQUENCY

Typical Performance Curves (Continued)

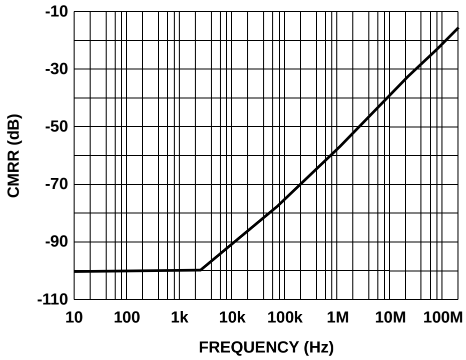


FIGURE 29. CMRR vs FREQUENCY

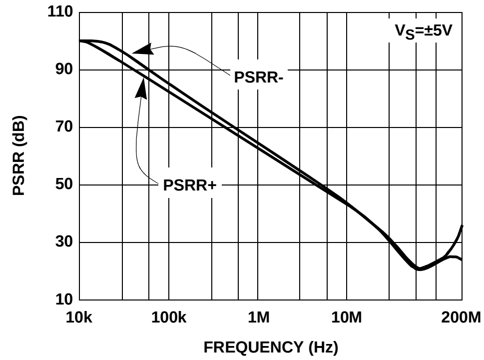


FIGURE 30. PSRR vs FREQUENCY

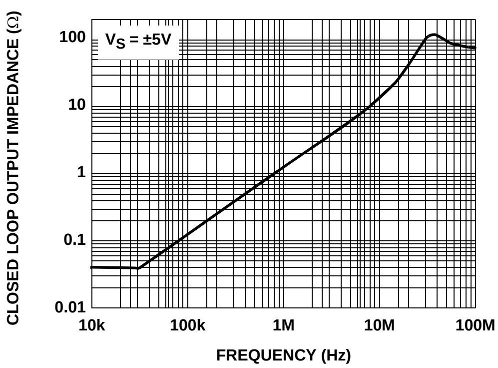


FIGURE 31. CLOSED LOOP OUTPUT IMPEDANCE vs FREQUENCY

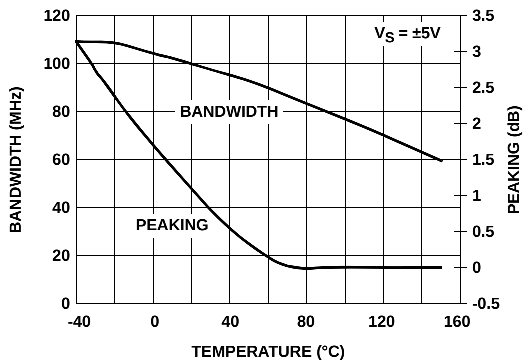


FIGURE 32. BANDWIDTH AND PEAKING vs TEMPERATURE

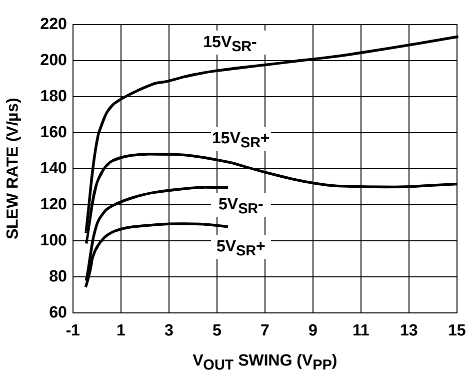


FIGURE 33. SLEW RATE vs SWING

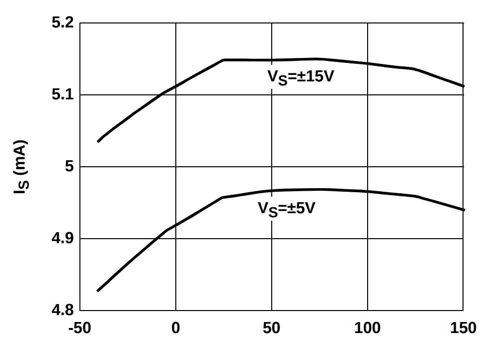


FIGURE 34. SUPPLY CURRENT vs TEMPERATURE

Typical Performance Curves (Continued)

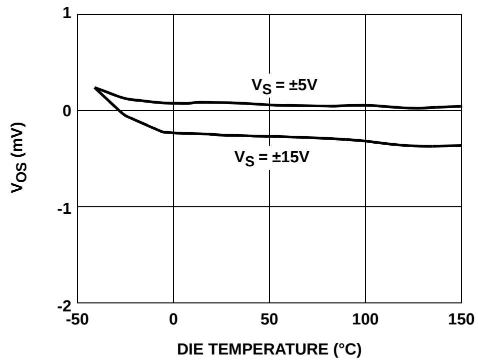


FIGURE 35. OFFSET VOLTAGE vs TEMPERATURE

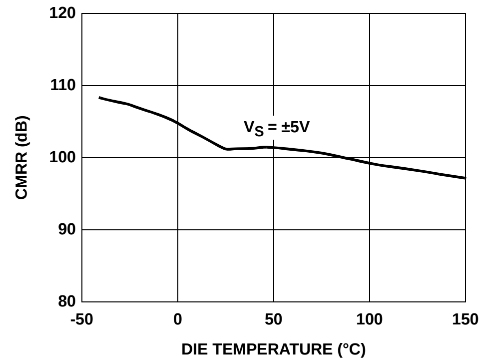


FIGURE 36. CMRR vs TEMPERATURE

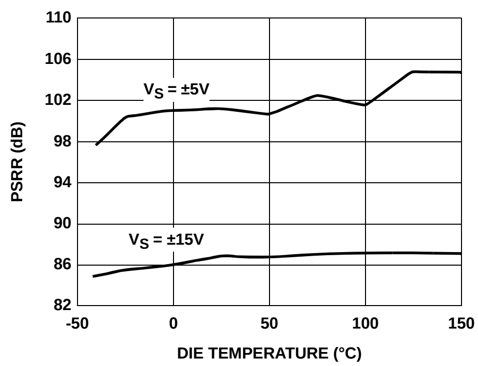


FIGURE 37. PSRR vs TEMPERATURE

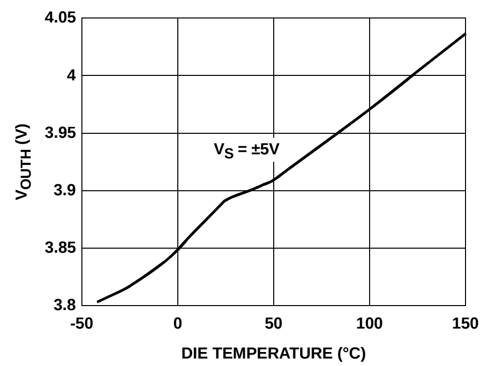


FIGURE 38. POSITIVE OUTPUT SWING vs TEMPERATURE

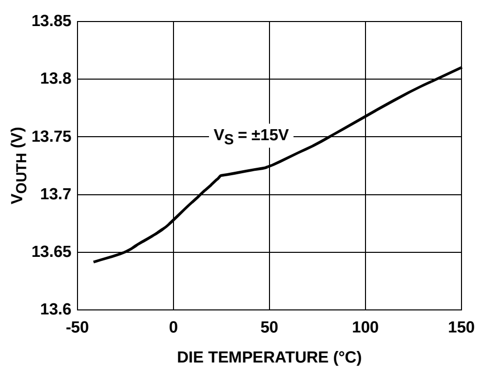


FIGURE 39. POSITIVE OUTPUT SWING vs TEMPERATURE

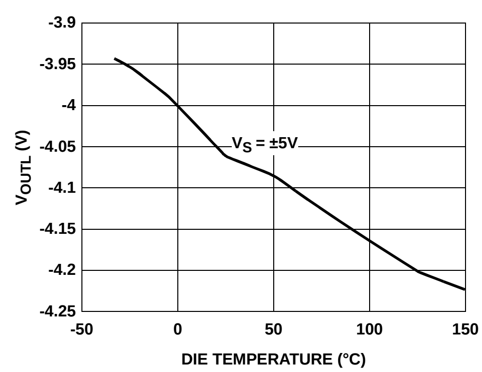


FIGURE 40. NEGATIVE OUTPUT SWING vs TEMPERATURE

Typical Performance Curves (Continued)

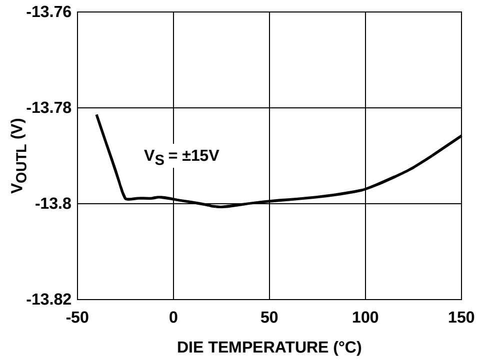


FIGURE 41. NEGATIVE OUTPUT SWING vs TEMPERATURE

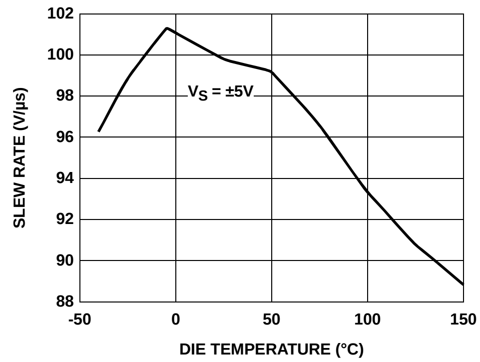


FIGURE 42. SLEW RATE vs TEMPERATURE

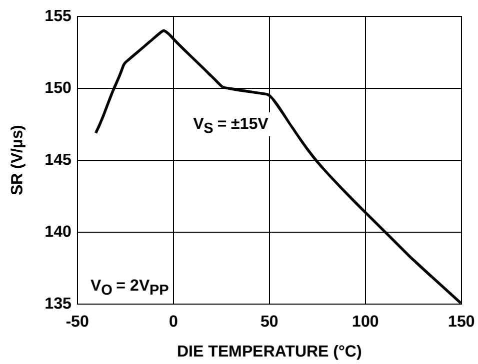


FIGURE 43. SLEW RATE vs TEMPERATURE

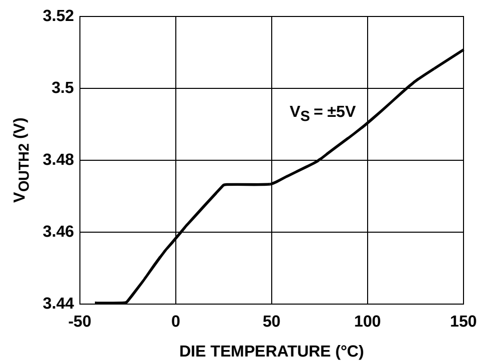


FIGURE 44. POSITIVE LOADED OUTPUT SWING vs TEMPERATURE

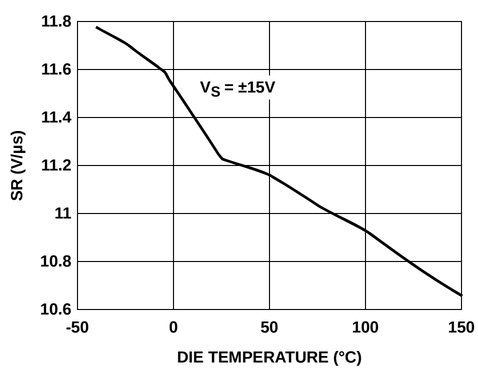


FIGURE 45. POSITIVE LOADED OUTPUT SWING vs TEMPERATURE

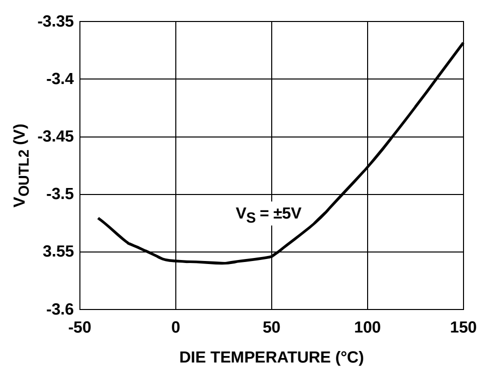


FIGURE 46. NEGATIVE LOADED OUTPUT SWING vs TEMPERATURE

Typical Performance Curves (Continued)

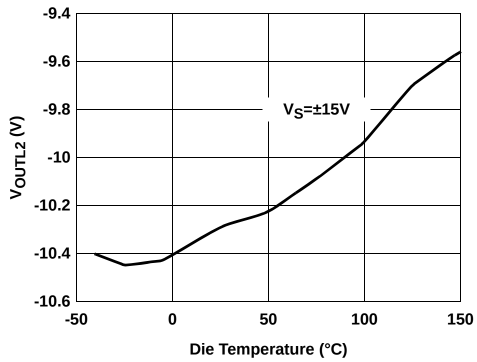


FIGURE 47. NEGATIVE LOADED OUTPUT SWING vs TEMPERATURE

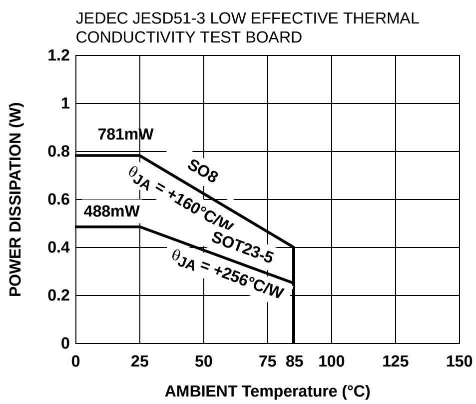


FIGURE 48. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

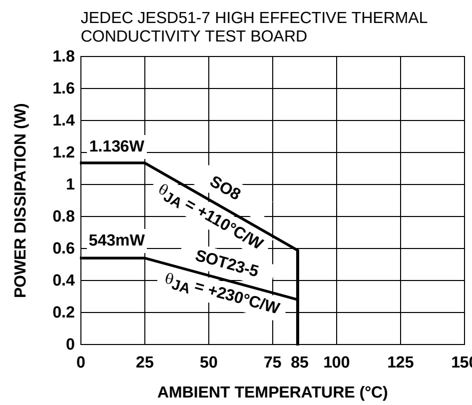
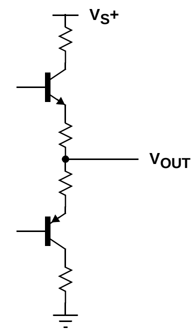
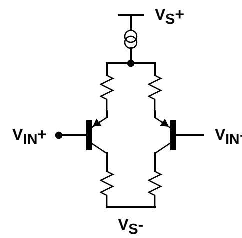


FIGURE 49. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

Pin Descriptions

EL2126CW (5 Ld SOT-23)	EL2126CS (8 Ld SOIC)	PIN NAME	PIN FUNCTION	EQUIVALENT CIRCUIT
1	6	VOUT	Output	 Circuit 1
2	4	VS-	Supply	
3	3	VINA+	Input	 Circuit 2
4	2	VINA-	Input	Reference Circuit 2
5	7	VS+	Supply	

Applications Information

Product Description

The EL2126 is an ultra-low noise, wideband monolithic operational amplifier built on Elantec's proprietary high speed complementary bipolar process. It features 1.3nV/√Hz input voltage noise, 200µV typical offset voltage, and 73dB THD. It is intended for use in systems such as ultrasound imaging where very small signals are needed to be amplified. The EL2126 also has excellent DC specifications: 200µV V_{OS}, 22µA IB, 0.4µA I_{OS}, and 106dB CMRR. These specifications allow the EL2126 to be used in DC-sensitive applications such as difference amplifiers.

Gain-Bandwidth Product

The EL2126 has a gain-bandwidth product of 650MHz at ±5V. For gains less than 20, higher-order poles in the amplifier's transfer function contribute to even higher closed-loop bandwidths. For example, the EL2126 has a -3dB bandwidth of 100MHz at a gain of 10 and decreases to 33MHz at gain of 20. It is important to note that the extra bandwidth at lower gain does not come at the expenses of stability. Even though the EL2126 is designed for gain ≥ 10. With external compensation, the device can also operate at lower gain settings. The RC network shown in Figure 50 reduces the feedback gain at high frequency and thus maintains the amplifier stability. R values must be less than RF divided by 9 and 1 divided by 2πRC must be less than 200MHz.

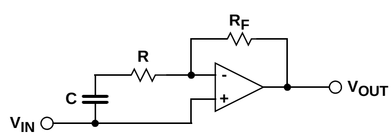


FIGURE 50.

Choice of Feedback Resistor, RF

The feedback resistor forms a pole with the input capacitance. As this pole becomes larger, phase margin is reduced. This increases ringing in the time domain and peaking in the frequency domain. Therefore, RF has some maximum value which should not be exceeded for optimum performance. If a large value of RF must be used, a small capacitor in the few pF range in parallel with RF can help to reduce this ringing and peaking at the expense of reducing the bandwidth. Frequency response curves for various RF values are shown in the typical performance curves section of this data sheet.

Noise Calculations

The primary application for the EL2126 is to amplify very small signals. To maintain the proper signal-to-noise ratio, it is essential to minimize noise contribution from the amplifier. Figure 51 shows all the noise sources for all the components around the amplifier.

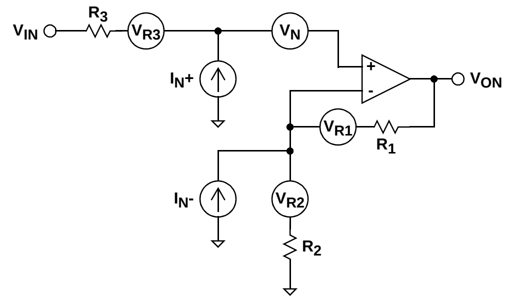


FIGURE 51.

V_N is the amplifier input voltage noise

I_N+ is the amplifier positive input current noise

I_N- is the amplifier negative input current noise

V_{RX} is the thermal noise associated with each resistor:

$$V_{RX} = \sqrt{4kTRx} \qquad \text{(EQ. 1)}$$

where:

k is Boltzmann's constant = 1.380658 x 10^{-23}

T is temperature in degrees Kelvin (273 + °C)

The total noise due to the amplifier seen at the output of the amplifier can be calculated by using the Equation 2.

As the equation shows, to keep noise at a minimum, small resistor values should be used. At higher amplifier gain configuration where R_2 is reduced, the noise due to IN-, R_2, and R_1 decreases and the noise caused by IN+, VN, and R_3 starts to dominate. Because noise is summed in a root-mean-squares method, noise sources smaller than 25% of the largest noise source can be ignored. This can greatly simplify the formula and make noise calculation much easier to calculate.

$$V_{ON} = \sqrt{BW} \times \sqrt{\left(VN^2 \times \left(1 + \frac{R_1}{R_2}\right)^2 + IN-^2 \times R_1^2 + IN+^2 \times R_3^2 \times \left(1 + \frac{R_1}{R_2}\right)^2 + 4 \times K \times T \times R_1 + 4 \times K \times T \times R_2 \times \left(\frac{R_1}{R_2}\right)^2 + 4 \times K \times T \times R_3 \times \left(1 + \frac{R_1}{R_2}\right)^2\right)}$$

(EQ. 2)

Output Drive Capability

The EL2126 is designed to drive low impedance load. It can easily drive $6V_{P-P}$ signal into a 100Ω load. This high output drive capability makes the EL2126 an ideal choice for RF, IF, and video applications. Furthermore, the EL2126 is current-limited at the output, allowing it to withstand momentary short to ground. However, the power dissipation with output-shorted cannot exceed the power dissipation capability of the package.

Driving Cables and Capacitive Loads

Although the EL2126 is designed to drive low impedance load, capacitive loads will decreases the amplifier's phase margin. As shown in the performance curves, capacitive load can result in peaking, overshoot and possible oscillation. For optimum AC performance, capacitive loads should be reduced as much as possible or isolated with a series resistor between 5Ω to 20Ω. When driving coaxial cables, double termination is always recommended for reflection-free performance. When properly terminated, the capacitance of the coaxial cable will not add to the capacitive load seen by the amplifier.

Power Supply Bypassing And Printed Circuit Board Layout

As with any high frequency devices, good printed circuit board layout is essential for optimum performance. Ground plane construction is highly recommended. Lead lengths should be kept as short as possible. The power supply pins must be closely bypassed to reduce the risk of oscillation. The combination of a 4.7µF tantalum capacitor in parallel with 0.1µF ceramic capacitor has been proven to work well when placed at each supply pin. For single supply operation, where pin 4 (V_S-) is connected to the ground plane, a single 4.7µF tantalum capacitor in parallel with a 0.1µF ceramic capacitor across pins 7 (V_S+) and pin 4 (V_S-) will suffice.

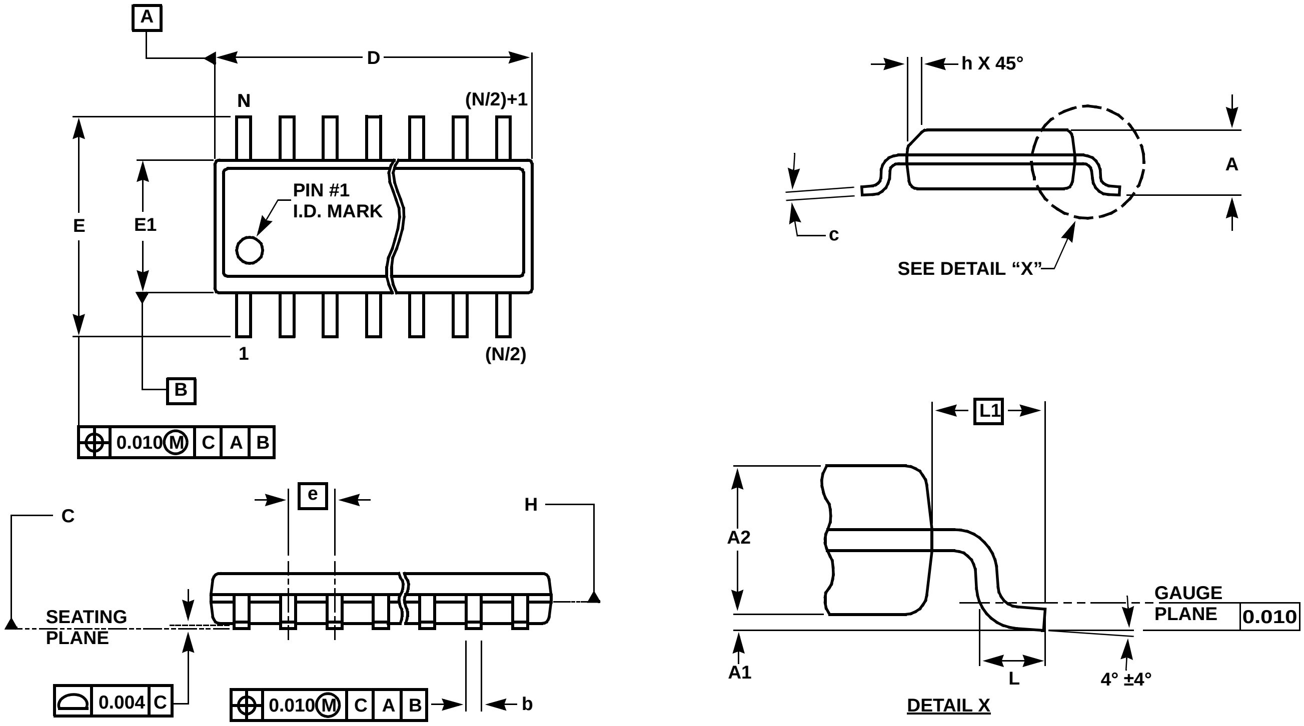
For good AC performance, parasitic capacitance should be kept to a minimum. Ground plane construction again should be used. Small chip resistors are recommended to minimize series inductance. Use of sockets should be avoided since they add parasitic inductance and capacitance which will result in additional peaking and overshoot.

Supply Voltage Range and Single Supply Operation

The EL2126 has been designed to operate with supply voltage range of ±2.5V to ±15V. With a single supply, the EL2126 will operate from +5V to +30V. Pins 4 and 7 are the power supply pins. The positive power supply is connected to pin 7. When used in single supply mode, pin 4 is connected to ground. When used in dual supply mode, the negative power supply is connected to pin 4.

As the power supply voltage decreases from +30V to +5V, it becomes necessary to pay special attention to the input voltage range. The EL2126 has an input voltage range of 0.4V from the negative supply to 1.2V from the positive supply. So, for example, on a single +5V supply, the EL2126 has an input voltage range which spans from 0.4V to 3.8V. The output range of the EL2126 is also quite large, on a +5V supply, it swings from 0.4V to 3.8V.

Small Outline Package Family (SO)



MDP0027

SMALL OUTLINE PACKAGE FAMILY (SO)

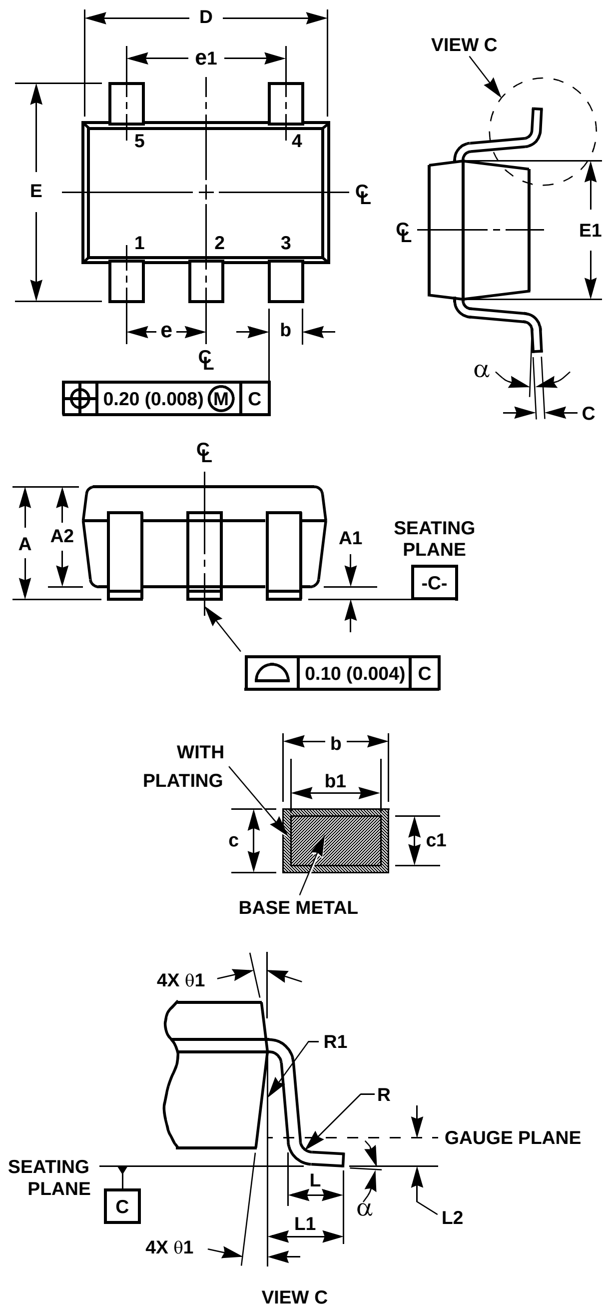
SYMBOL	INCHES							TOLERANCE	NOTES
	SO-8	SO-14	SO16 (0.150")	SO16 (0.300") (SOL-16)	SO20 (SOL-20)	SO24 (SOL-24)	SO28 (SOL-28)		
A	0.068	0.068	0.068	0.104	0.104	0.104	0.104	MAX	-
A1	0.006	0.006	0.006	0.007	0.007	0.007	0.007	±0.003	-
A2	0.057	0.057	0.057	0.092	0.092	0.092	0.092	±0.002	-
b	0.017	0.017	0.017	0.017	0.017	0.017	0.017	±0.003	-
c	0.009	0.009	0.009	0.011	0.011	0.011	0.011	±0.001	-
D	0.193	0.341	0.390	0.406	0.504	0.606	0.704	±0.004	1, 3
E	0.236	0.236	0.236	0.406	0.406	0.406	0.406	±0.008	-
E1	0.154	0.154	0.154	0.295	0.295	0.295	0.295	±0.004	2, 3
e	0.050	0.050	0.050	0.050	0.050	0.050	0.050	Basic	-
L	0.025	0.025	0.025	0.030	0.030	0.030	0.030	±0.009	-
L1	0.041	0.041	0.041	0.056	0.056	0.056	0.056	Basic	-
h	0.013	0.013	0.013	0.020	0.020	0.020	0.020	Reference	-
N	8	14	16	16	20	24	28	Reference	-

Rev. M 2/07

NOTES:

1. Plastic or metal protrusions of 0.006" maximum per side are not included.
2. Plastic interlead protrusions of 0.010" maximum per side are not included.
3. Dimensions "D" and "E1" are measured at Datum Plane "H".
4. Dimensioning and tolerancing per ASME Y14.5M-1994

Small Outline Transistor Plastic Packages (SOT23-5)



P5.064

5 LEAD SMALL OUTLINE TRANSISTOR PLASTIC PACKAGE

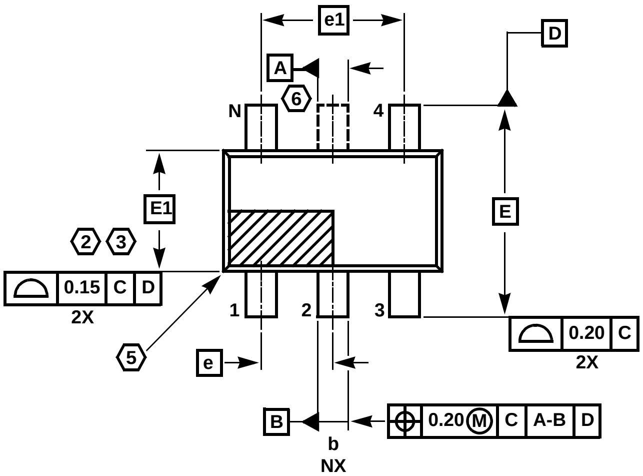
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.036	0.057	0.90	1.45	-
A1	0.000	0.0059	0.00	0.15	-
A2	0.036	0.051	0.90	1.30	-
b	0.012	0.020	0.30	0.50	-
b1	0.012	0.018	0.30	0.45	
c	0.003	0.009	0.08	0.22	6
c1	0.003	0.008	0.08	0.20	6
D	0.111	0.118	2.80	3.00	3
E	0.103	0.118	2.60	3.00	-
E1	0.060	0.067	1.50	1.70	3
e	0.0374 Ref		0.95 Ref		-
e1	0.0748 Ref		1.90 Ref		-
L	0.014	0.022	0.35	0.55	4
L1	0.024 Ref.		0.60 Ref.		
L2	0.010 Ref.		0.25 Ref.		
N	5		5		5
R	0.004	-	0.10	-	
R1	0.004	0.010	0.10	0.25	
α	0^{o}	8^{o}	0^{o}	8^{o}	-

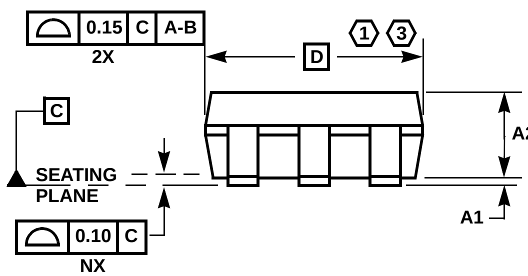
Rev. 2 9/03

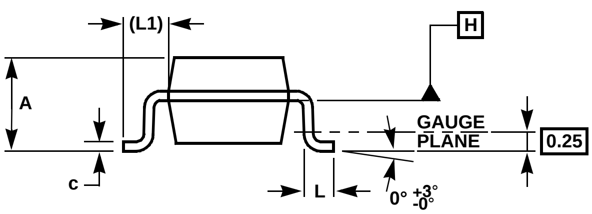
NOTES:

1. Dimensioning and tolerance per ASME Y14.5M-1994.
2. Package conforms to EIAJ SC-74 and JEDEC MO178AA.
3. Dimensions D and E1 are exclusive of mold flash, protrusions, or gate burrs.
4. Footlength L measured at reference to gauge plane.
5. “N” is the number of terminal positions.
6. These Dimensions apply to the flat section of the lead between 0.08mm and 0.15mm from the lead tip.
7. Controlling dimension: MILLIMETER. Converted inch dimensions are for reference only.

SOT-23 Package Family







MDP0038

SOT-23 PACKAGE FAMILY

SYMBOL	MILLIMETERS		TOLERANCE
	SOT23-5	SOT23-6	
A	1.45	1.45	MAX
A1	0.10	0.10	±0.05
A2	1.14	1.14	±0.15
b	0.40	0.40	±0.05
c	0.14	0.14	±0.06
D	2.90	2.90	Basic
E	2.80	2.80	Basic
E1	1.60	1.60	Basic
e	0.95	0.95	Basic
e1	1.90	1.90	Basic
L	0.45	0.45	±0.10
L1	0.60	0.60	Reference
N	5	6	Reference

Rev. F 2/07

NOTES:

1. Plastic or metal protrusions of 0.25mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25mm maximum per side are not included.
3. This dimension is measured at Datum Plane “H”.
4. Dimensioning and tolerancing per ASME Y14.5M-1994.
5. Index area - Pin #1 I.D. will be located within the indicated zone (SOT23-6 only).
6. SOT23-5 version has no center lead (shown as a dashed line).